FIG. 1

FIG. 2

START

PERFORM BIT ALLOCATION
BY KNOWN METHOD ─ 501

CALCULATE TOTAL
BIT COUNT b_base ─ 502

CHECK RANGE #n_max_1 to
#n_max_k OF CARRIERS TO
WHICH BITS OF MAXIMUM NUMBER ─ 503
HAVE BEEN ALLOCATED

DECREASE POWERS OF CARRIERS
#n_max_1 to #n_max_k BY Δx ─ 504
(MAKING TOTAL POWER
DECREASE EQUAL TO $k \cdot \Delta x$)

INCREASE POWERS OF CARRIERS
HAVING LARGE NUMBERS OF
ALLOCATED BITS UP TO TOTAL ─ 505
POWER OF $k \cdot \Delta x$

CALCULATE SUM TOTAL b_sum
OF NUMBERS OF BITS ─ 506

509

REDUCE NUMBER k OF
CARRIERS OF INTEREST

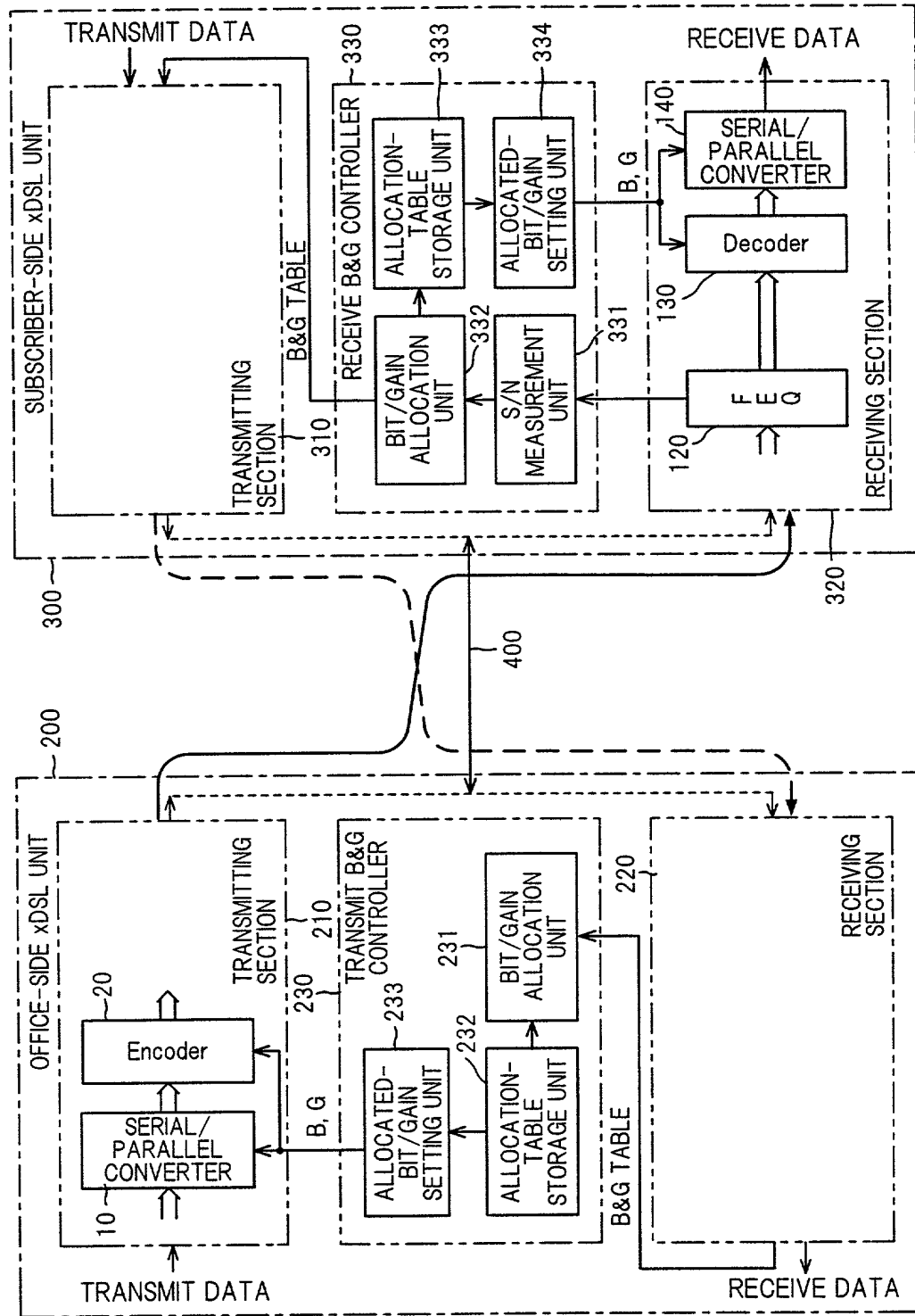507

b_sum>b_base ?   NO

YES or k=0

DECIDE ─ 508

END

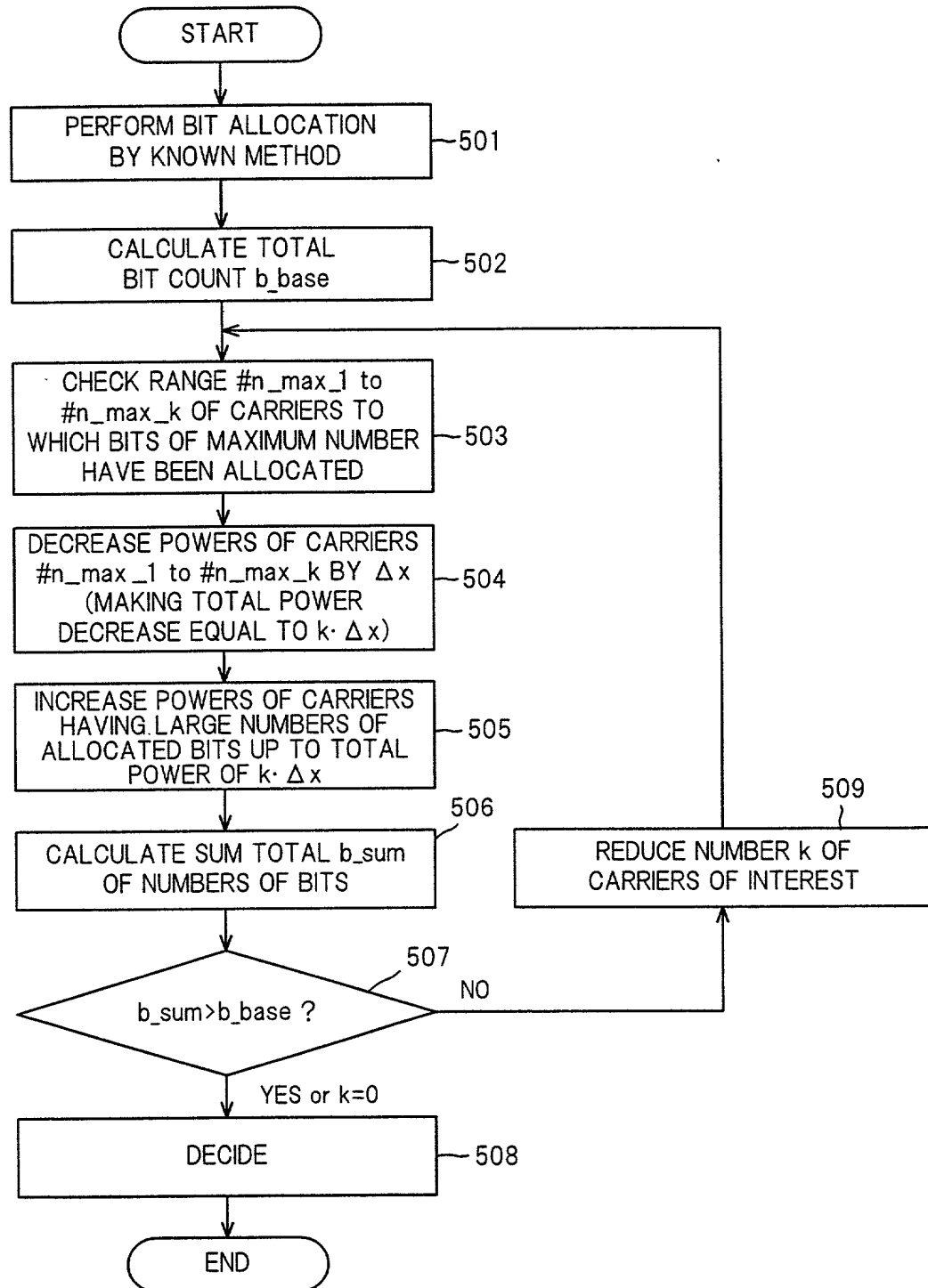## FIG. 3

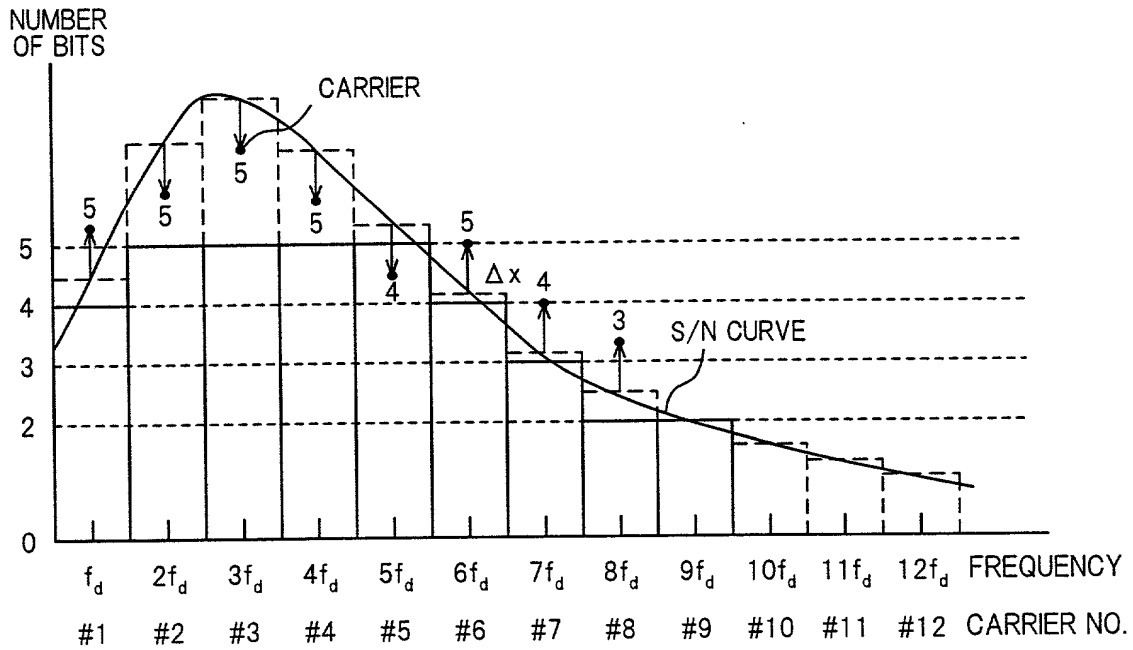## FIG. 4

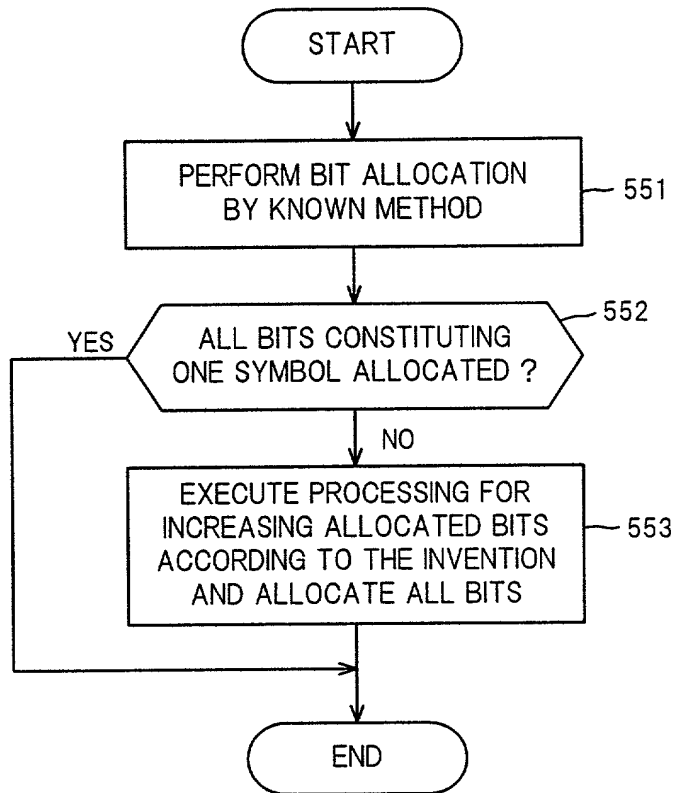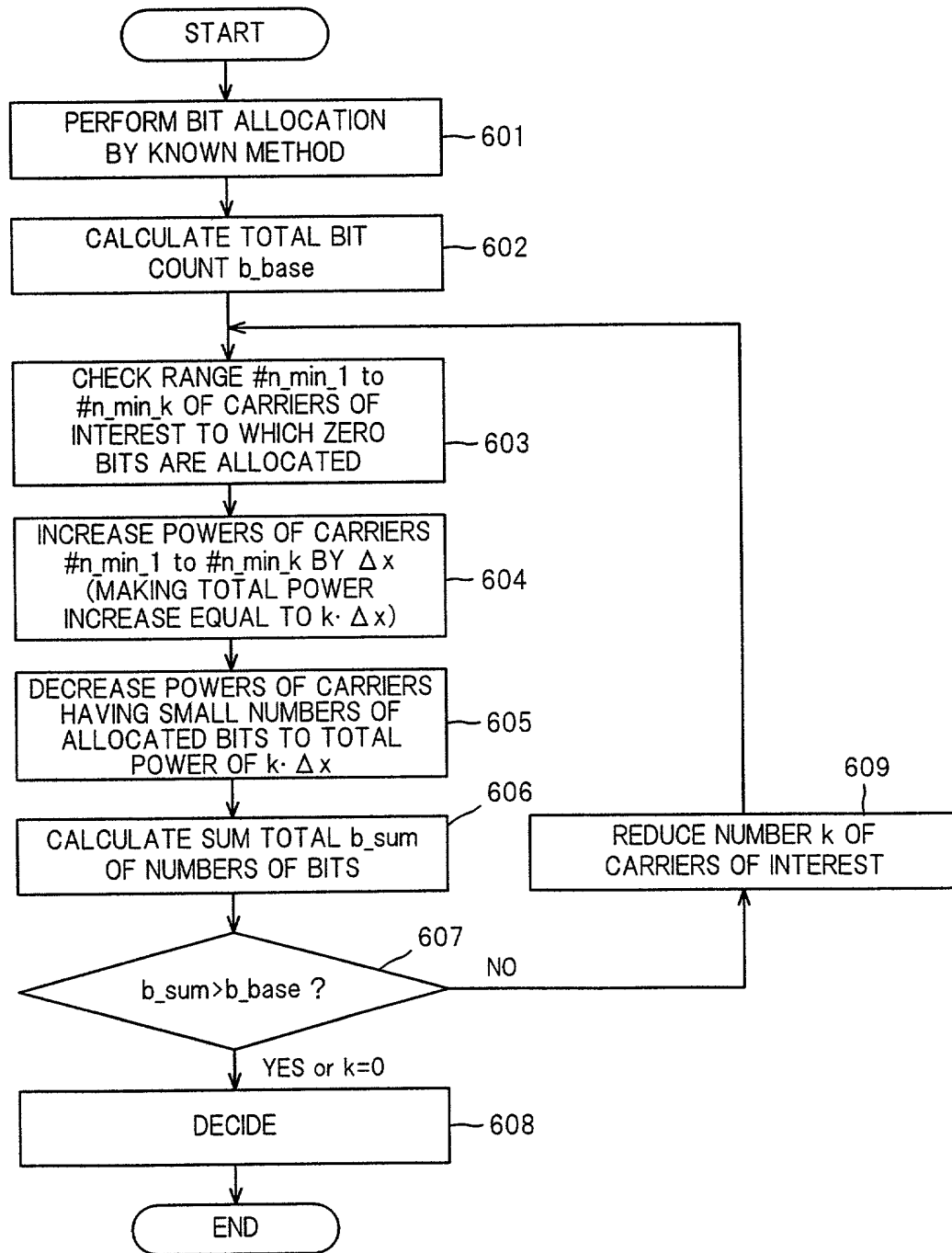| NO.	1	2	3	4	5	6	7	8	9	10	11	12	TOTAL
BITS	5	5	5	5	4	5	4	3	2	0	0	0	38
ADDITIONAL GAIN	$+\Delta x$	$-\Delta x$	$-\Delta x$	$-\Delta x$	$-\Delta x$	$+\Delta x$	$+\Delta x$	$+\Delta x$	0	0	0	0	0

FIG. 5

START

PERFORM BIT ALLOCATION
BY KNOWN METHOD — 551

ALL BITS CONSTITUTING
ONE SYMBOL ALLOCATED ? — 552

YES

NO

EXECUTE PROCESSING FOR
INCREASING ALLOCATED BITS
ACCORDING TO THE INVENTION — 553
AND ALLOCATE ALL BITS

END

FIG. 6

START

PERFORM BIT ALLOCATION BY KNOWN METHOD — 601

CALCULATE TOTAL BIT COUNT b_base — 602

CHECK RANGE #n_min_1 to #n_min_k OF CARRIERS OF INTEREST TO WHICH ZERO BITS ARE ALLOCATED — 603

INCREASE POWERS OF CARRIERS #n_min_1 to #n_min_k BY Δx (MAKING TOTAL POWER INCREASE EQUAL TO $k \cdot \Delta x$) — 604

DECREASE POWERS OF CARRIERS HAVING SMALL NUMBERS OF ALLOCATED BITS TO TOTAL POWER OF $k \cdot \Delta x$ — 605

CALCULATE SUM TOTAL b_sum OF NUMBERS OF BITS — 606

607 — b_sum>b_base ?

NO

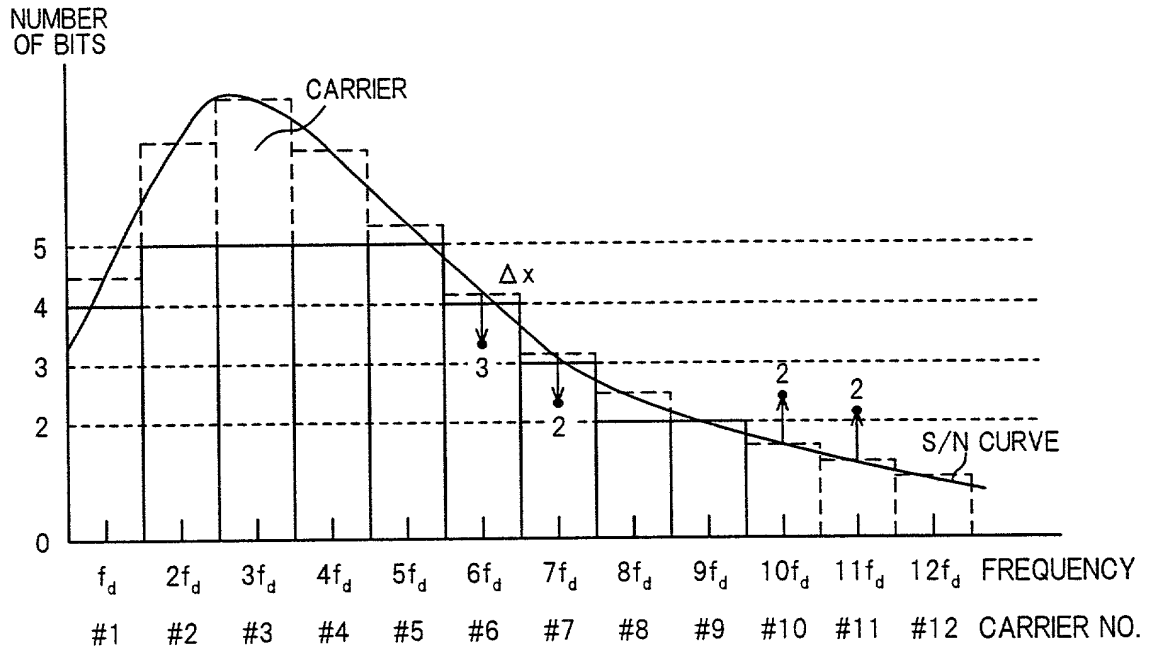609 — REDUCE NUMBER k OF CARRIERS OF INTEREST

YES or k=0

DECIDE — 608

END

FIG. 7

FIG. 8

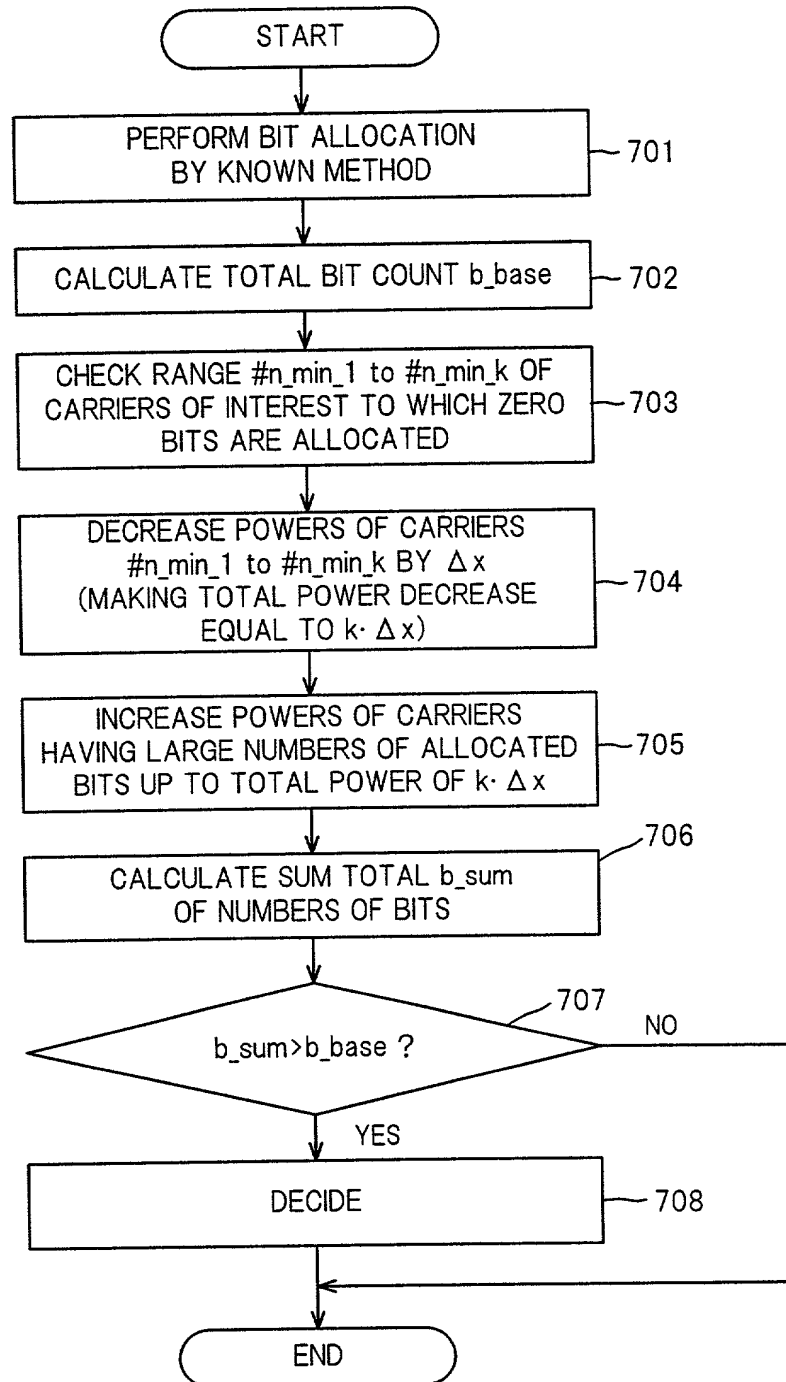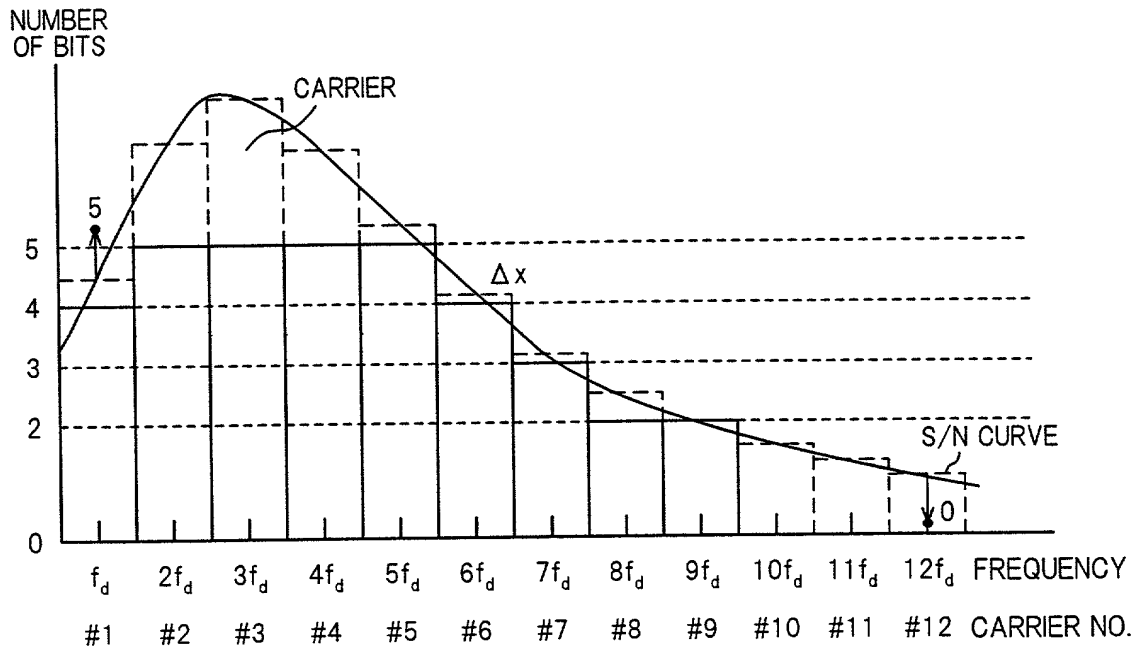| NO.	1	2	3	4	5	6	7	8	9	10	11	12	TOTAL
BITS	4	5	5	5	5	3	2	2	2	2	2	0	37
ADDITIONAL GAIN	0	0	0	0	0	$-\Delta x$	$-\Delta x$	0	0	$+\Delta x$	$+\Delta x$	0	0

FIG. 9

```
          ┌─────────────┐
          │    START    │
          └─────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │   PERFORM BIT ALLOCATION │────701
    │      BY KNOWN METHOD     │
    └──────────────────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │ CALCULATE TOTAL BIT COUNT b_base │────702
    └──────────────────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │ CHECK RANGE #n_min_1 to #n_min_k OF │
    │ CARRIERS OF INTEREST TO WHICH ZERO  │────703
    │      BITS ARE ALLOCATED             │
    └──────────────────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │  DECREASE POWERS OF CARRIERS │
    │   #n_min_1 to #n_min_k BY Δx │
    │  (MAKING TOTAL POWER DECREASE│────704
    │      EQUAL TO k· Δx)         │
    └──────────────────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │  INCREASE POWERS OF CARRIERS │
    │ HAVING LARGE NUMBERS OF ALLOCATED │────705
    │ BITS UP TO TOTAL POWER OF k· Δx   │
    └──────────────────────────┘
                 │
                 ▼
    ┌──────────────────────────┐
    │   CALCULATE SUM TOTAL b_sum │────706
    │     OF NUMBERS OF BITS      │
    └──────────────────────────┘
                 │
                 ▼
         ◇───────────────◇
         │ b_sum>b_base ? │────707      NO
         ◇───────────────◇ ─────────────┐
                 │                        │
                YES                       │
                 ▼                        │
    ┌──────────────────────────┐          │
    │          DECIDE          │────708   │
    └──────────────────────────┘          │
                 │                        │
                 ◄────────────────────────┘
                 ▼
          ┌─────────────┐
          │     END     │
          └─────────────┘
```

FIG. 10

FIG. 11

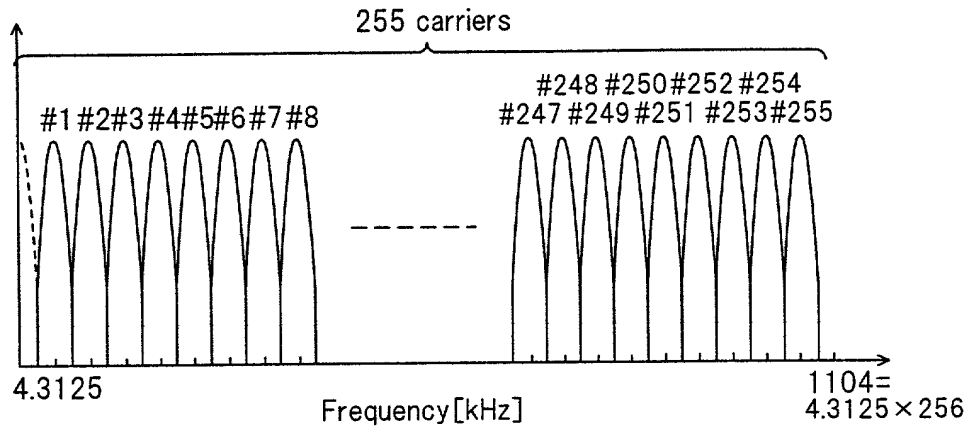| NO.	1	2	3	4	5	6	7	8	9	10	11	12	TOTAL
BITS	5	5	5	5	5	4	3	2	2	0	0	0	36
ADDITIONAL GAIN	$+\Delta x$	0	0	0	0	0	0	0	0	0	0	$-\Delta x$	0

FIG. 12 PRIOR ART

255 carriers

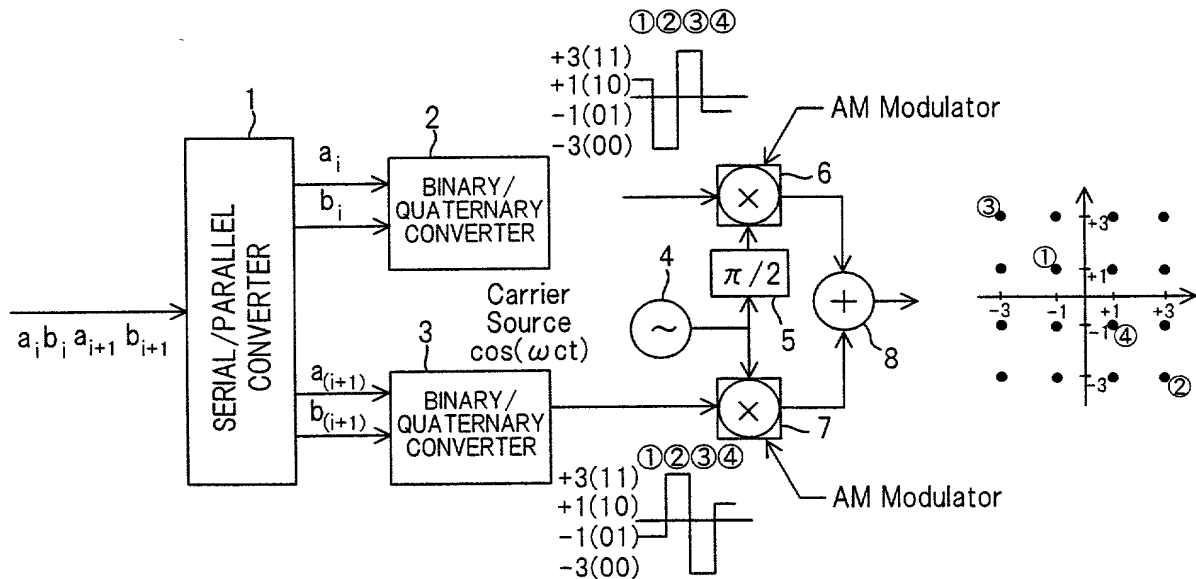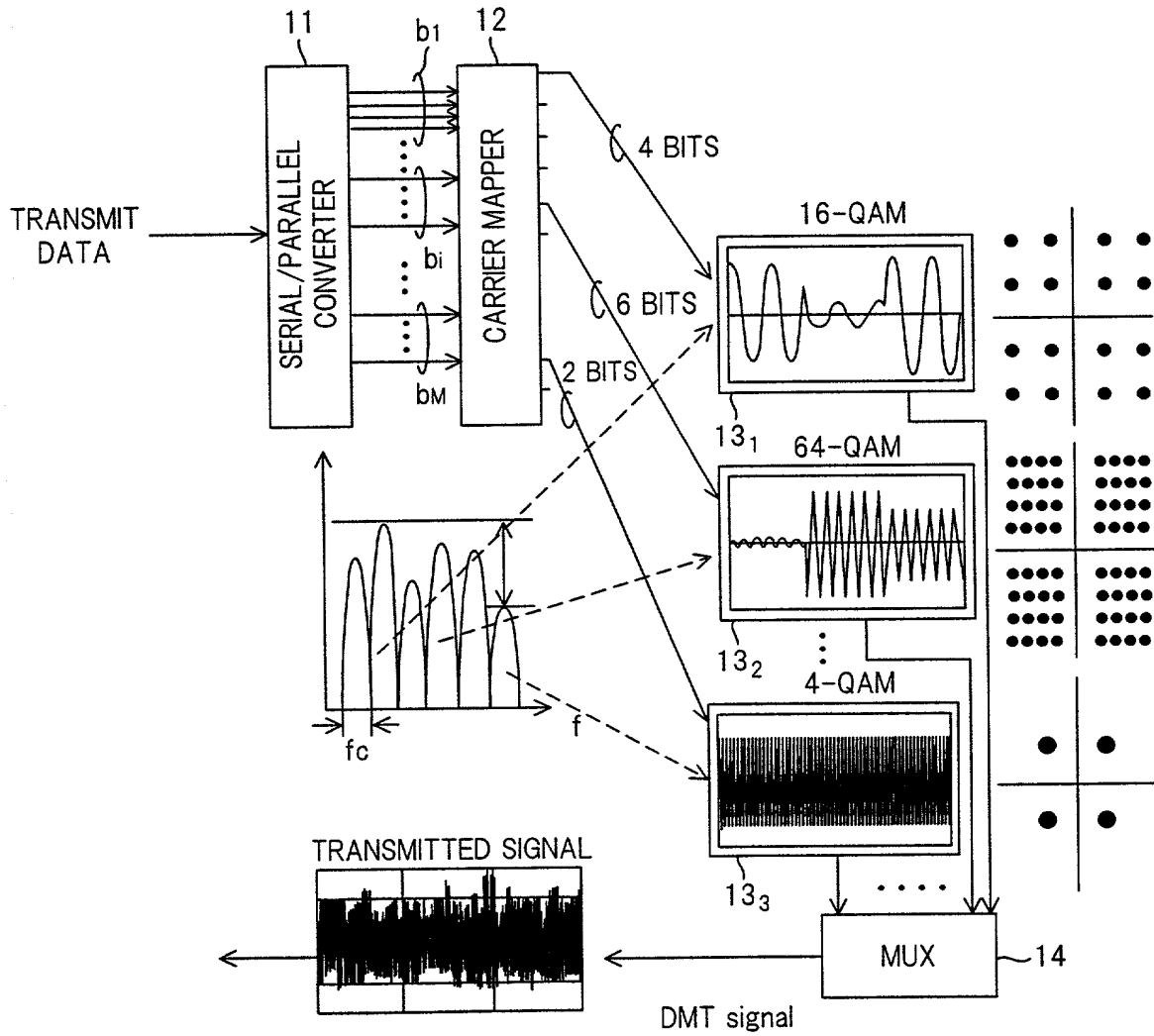#1#2#3#4#5#6#7#8

#248 #250#252#254
#247 #249#251 #253#255

4.3125

1104=
4.3125×256

Frequency[kHz]

FIG. 13 PRIOR ART

①②③④

+3(11)
+1(10)
−1(01)
−3(00)

AM Modulator

6

4

π/2

5

8

Carrier
Source
cos(ωct)

7

AM Modulator

+3(11) ①②③④
+1(10)
−1(01)
−3(00)

$a_i b_i a_{i+1} b_{i+1}$

SERIAL/PARALLEL CONVERTER

a_i
b_i

BINARY/
QUATERNARY
CONVERTER

$a_{(i+1)}$
$b_{(i+1)}$

BINARY/
QUATERNARY
CONVERTER

1

2

3

③   +3
①   +1
−3 −1   +1 +3
④
−3
②

FIG. 14 PRIOR ART

TRANSMIT DATA

11 SERIAL/PARALLEL CONVERTER

b_1

12 CARRIER MAPPER

b_i

b_M

4 BITS

6 BITS

2 BITS

16-QAM

13_1

64-QAM

13_2

4-QAM

13_3

f_c

f

TRANSMITTED SIGNAL

MUX ~14

DMT signal

FIG. 16 PRIOR ART

OFFICE SIDE

ADSL

ATU-C

①

③

④

SUBSCRIBER SIDE

ADSL

②
S/N RATIO
CALCULATION

ATU-R

FIG. 15 PRIOR ART

FIG. 17 PRIOR ART
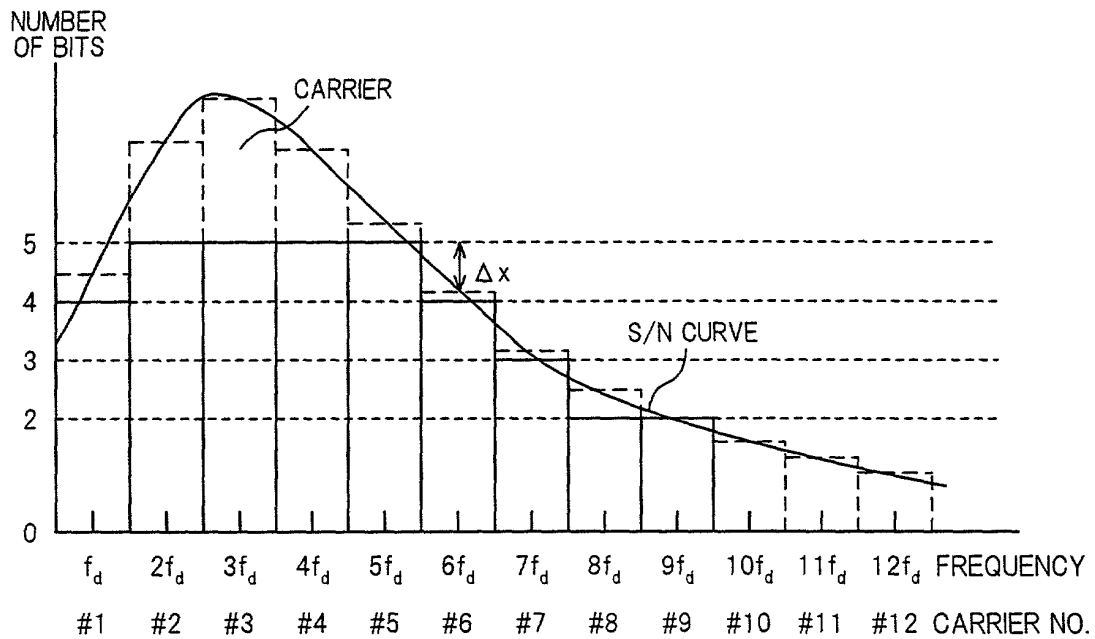
FIG. 18 PRIOR ART

NUMBERS OF BITS ALLOCATED BY BIT ALLOCATION BASED UPON KNOWN METHOD

CARRIER NO.	1	2	3	4	5	6	7	8	9	10	11	12	TOTAL
BITS	4	5	5	5	5	4	3	2	2	0	0	0	35